CHIP TESTING WITHIN A MULTI-CHIP SEMICONDUCTOR PACKAGE

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ABSTRACT OF THE INVENTION

A system and method is provided for testing a secondary chip housed within a multi-chip packaged semiconductor device. The packaged semiconductor device includes a secondary chip and a primary chip, with the secondary chip communicating with the primary chip through signal drivers. The secondary chip also includes at least one test signal driver connected to the signal drivers and to certain external connectors that may be shared with the primary chip. The test signal drivers provide testing of the secondary chip using standard integrated circuit test equipment while the secondary chip is contained within the packaged semiconductor device.